ABSTRACT OF THE DISCLOSURE

In a semiconductor device having an SOI structure and a method of manufacturing the same, influence by a parasitic transistor can be prevented, and no disadvantage is caused in connection with a manufacturing process. In this semiconductor device, an upper side portion of a semiconductor layer is rounded. Thereby, concentration of an electric field at the upper side portion of the semiconductor layer can be prevented. As a result, lowering of a threshold voltage of a parasitic transistor can be prevented, so that the parasitic transistor does not adversely affect subthreshold characteristics of a regular transistor. Owing to provision of a concavity of a U-shaped section, generation of etching residue can be prevented when etching a gate electrode for patterning the same. Thereby, a disadvantage is not caused in connection with the manufacturing process.